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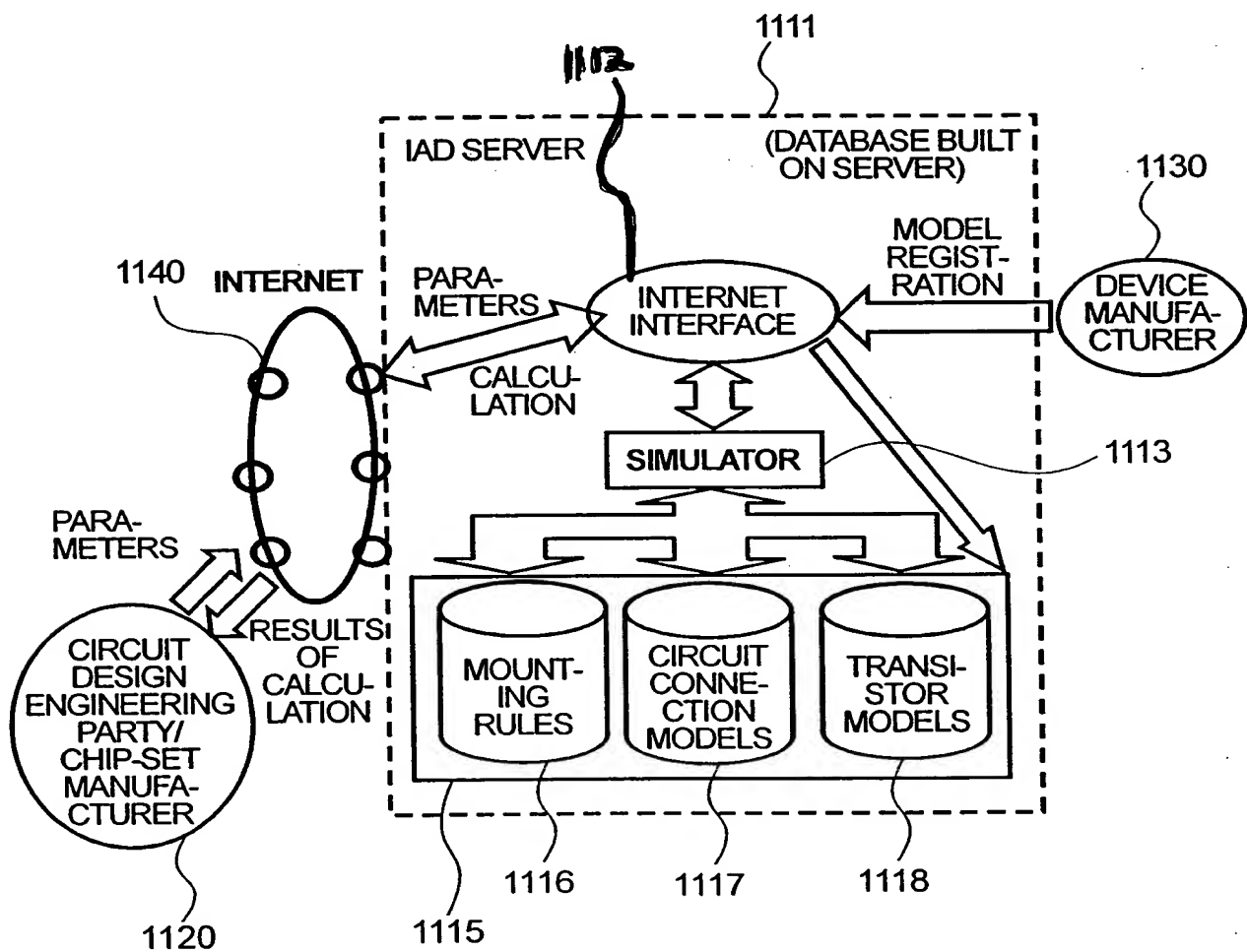
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3910  
10/10/00  
NEW DEPARTMENT

**FIG.1**  
SYSTEM CONFIGURATION



INVENTOR'S CERTIFICATE  
NO. 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

**FIG.3**  
EXAMPLE OF ENTRY SCREEN

## *Welcome to Web PCB Simulation*

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Last Modified at December 13, 2000

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- Circuits Simulation on WEB
- SPICE - JAVAscript / CGI connection technology
- SPICE transistor model available
- IBIS also available
- Transmission line analysis
- Signal Integrity analysis
- EMC simulation

---

Please Select the Circuit model

1. Single Transmission Line
2. Differential Signal Lines
3. Bus Lines
4. Crosstalk
5. EMC Noise
6. Switching Noise
7. others

**FIG.4**

EXAMPLE OF USER REGISTRATION

**Welcome to**  
**Web PCB Simulation**

Last Modified at December 13, 2000

- Circuits Simulation on WEB
- SPICE - JavaScript / CGI connection technology
- SPICE transistor model available
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- Transmission line analysis
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- EMC simulation

Please Select the Circuit model

1. Single Transmission Line
2. Differential Signal Lines
3. Bus Lines
4. Crosstalk
5. EMC Noise
6. Switching Noise
7. others

Input username and password

Enter a user name for Barong

User name:

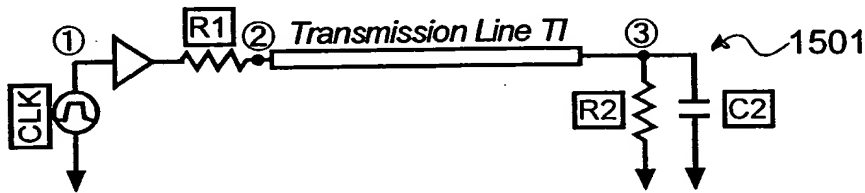
Password:

1405

1300

**FIG.5**  
EXAMPLE OF CIRCUIT  
PARAMETER INPUT SCREEN

Web SPICE - Spider -

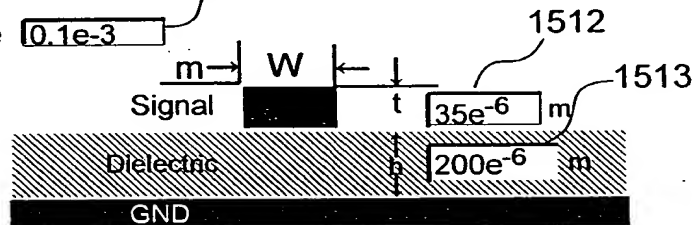


Set the parameters below.

- Clock CLK  MHz ~ 1502
- Transceiver TX  ~ 1503
- Resistor R1   $\Omega$  ~ 1504
- Resistor R2   $\Omega$  ~ 1505
- Capacitor C2  F ~ 1506
- Transmission Line

Line Type : ☒ Microstrip Line  ~ 1511

Line length  mm ~ 1516



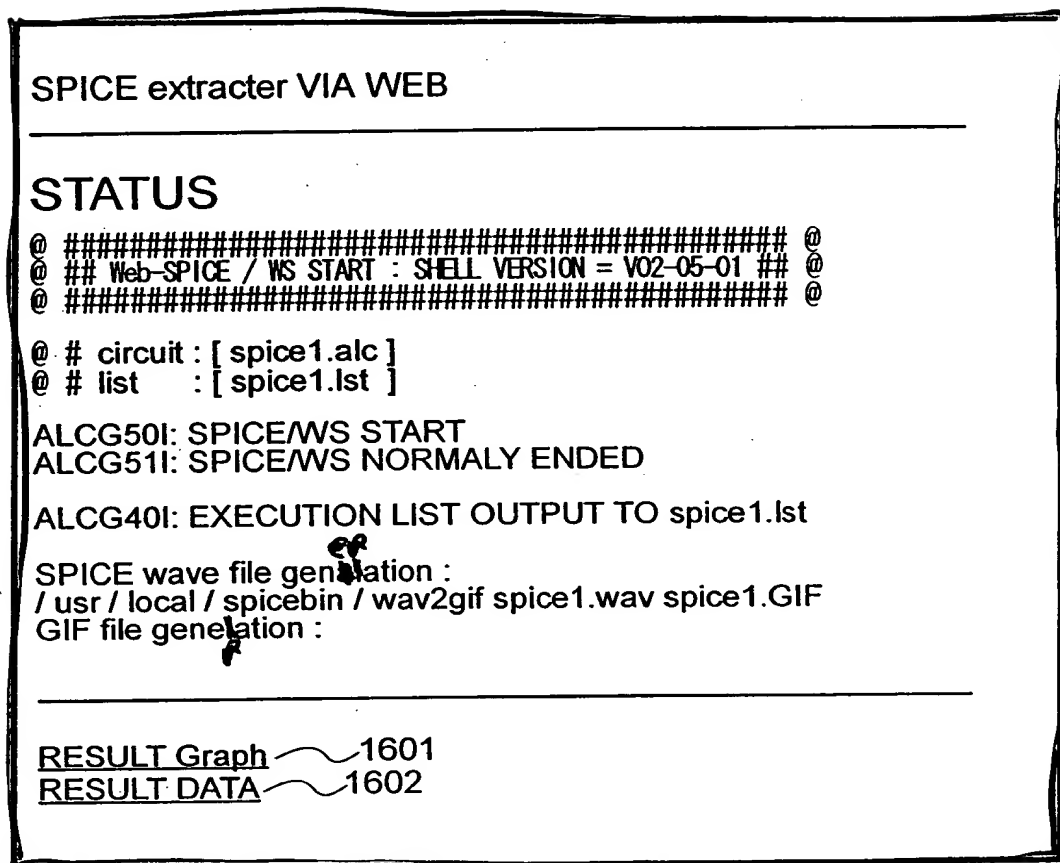
Dielectric Constant  $\epsilon_r$   ~ 1514

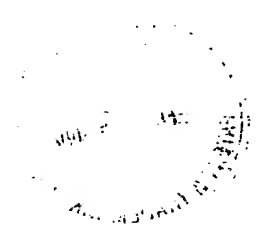
Permeability  $\mu_r$   ~ 1515

GO!(SPICE) ~ 1520

**FIG.6**

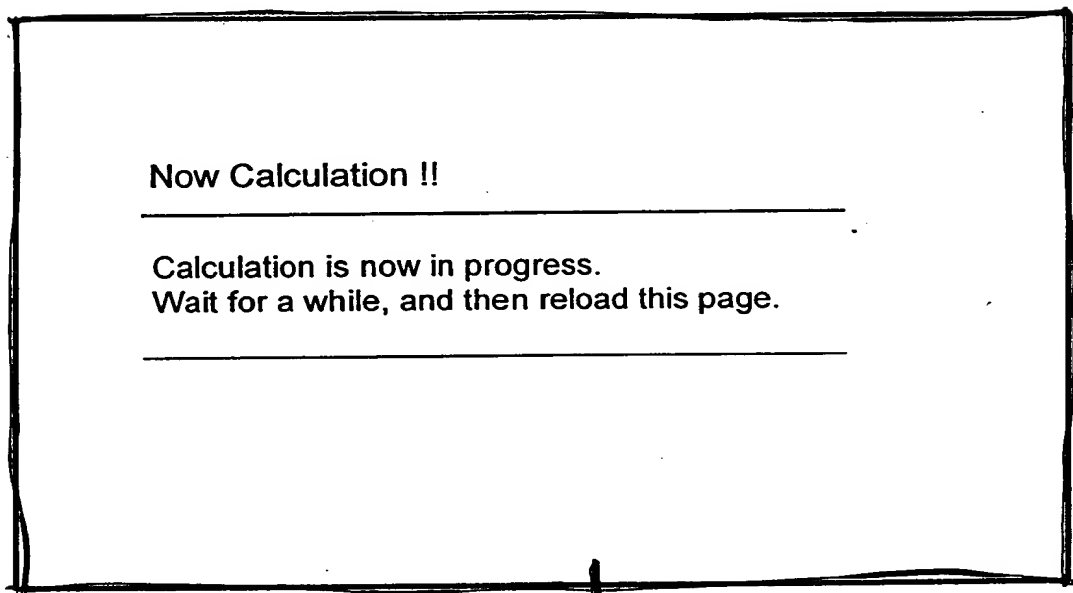
EXAMPLE OF CALCULATION STATUS SCREEN





## FIG.7

EXAMPLE OF CALCULATION RESULT SCREEN  
DISPLAYED IN THE COURSE OF CALCULATION



Now Calculation !!

---

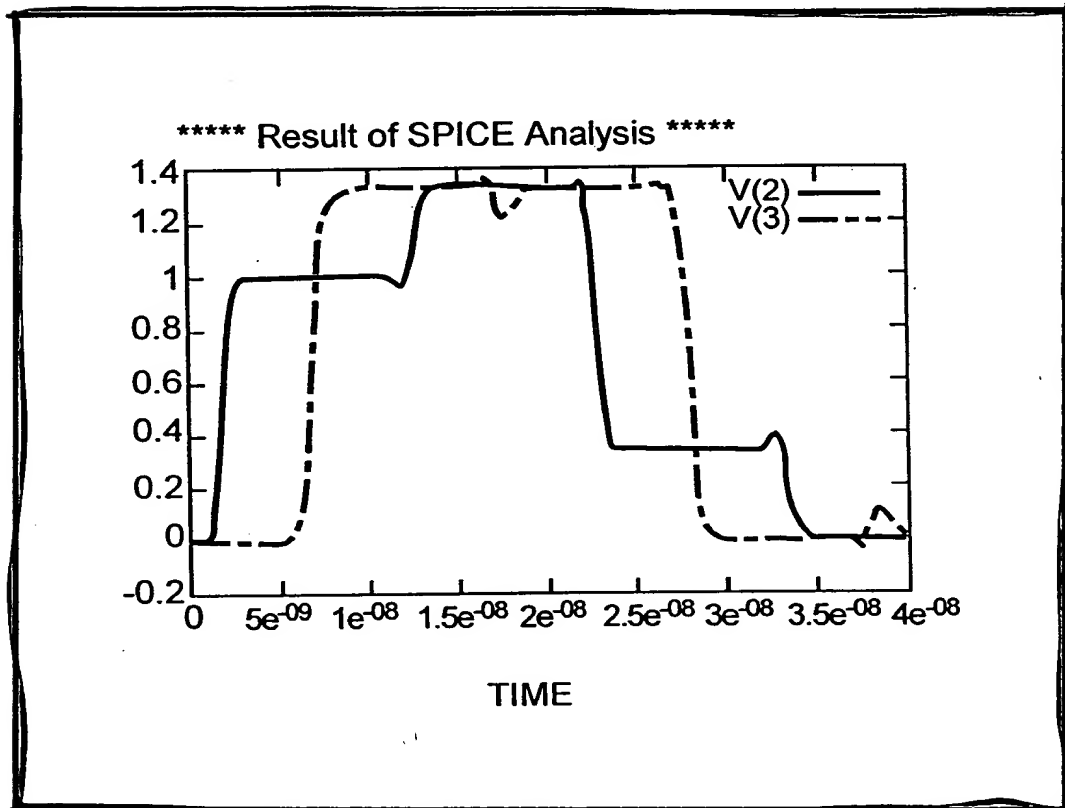
Calculation is now in progress.  
Wait for a while, and then reload this page.

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1704

**FIG.8**

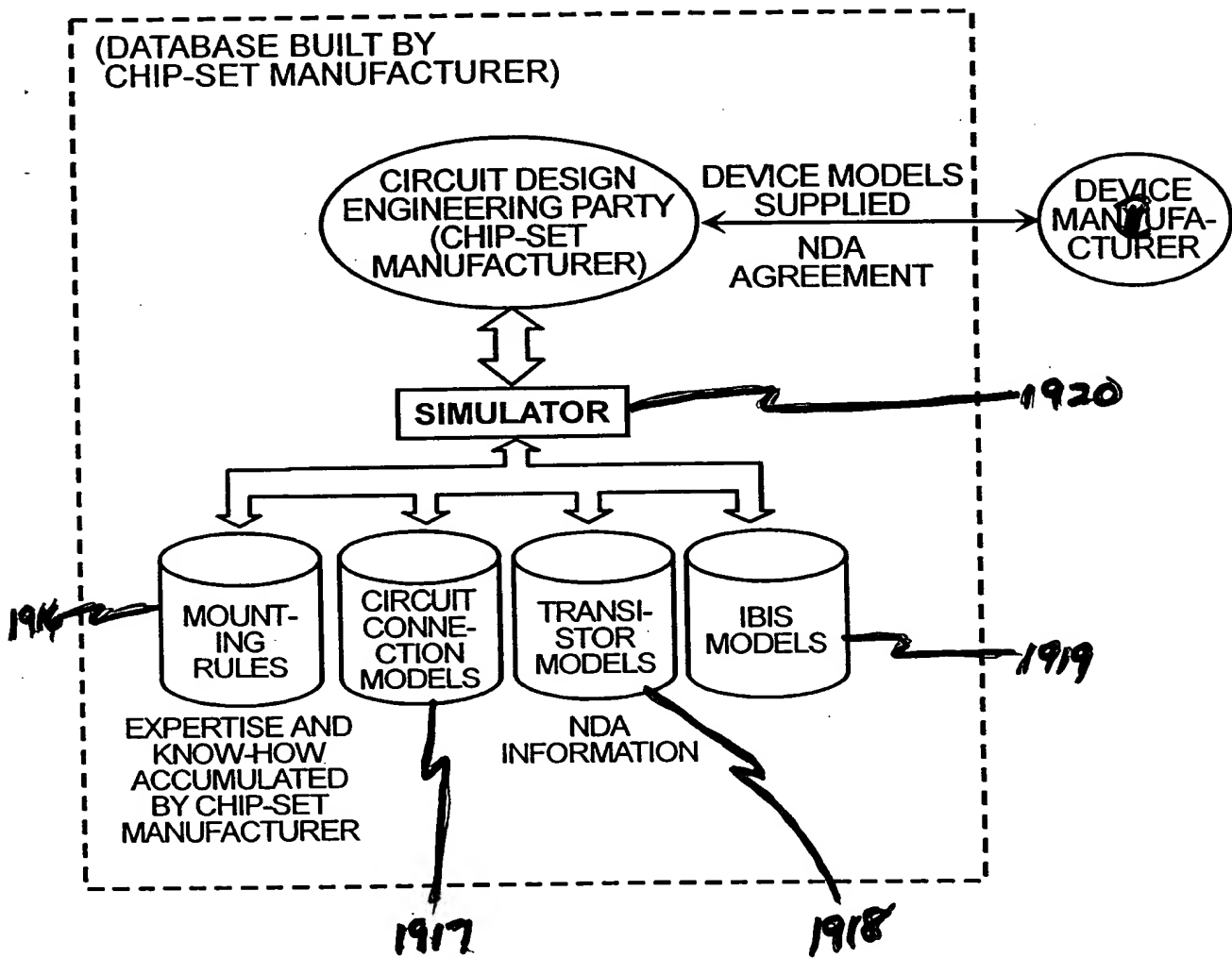
EXAMPLE OF CALCULATION RESULT  
SCREEN DISPLAYED AT THE END OF CALCULATION





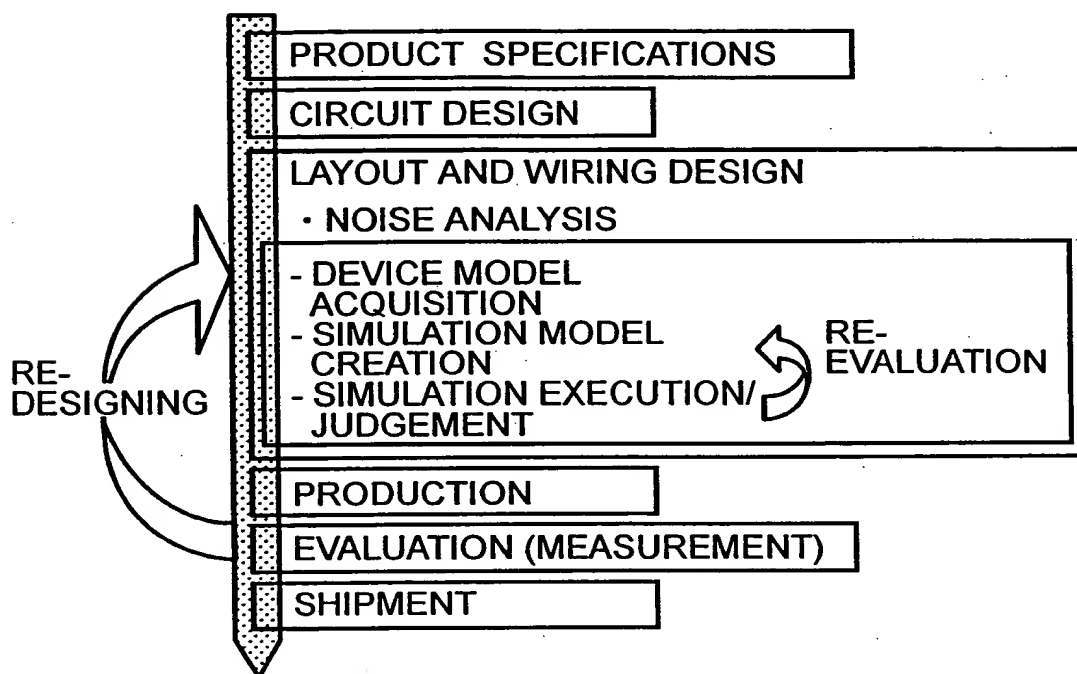
# FIG.9

## CONVENTIONAL SYSTEM CONFIGURATION



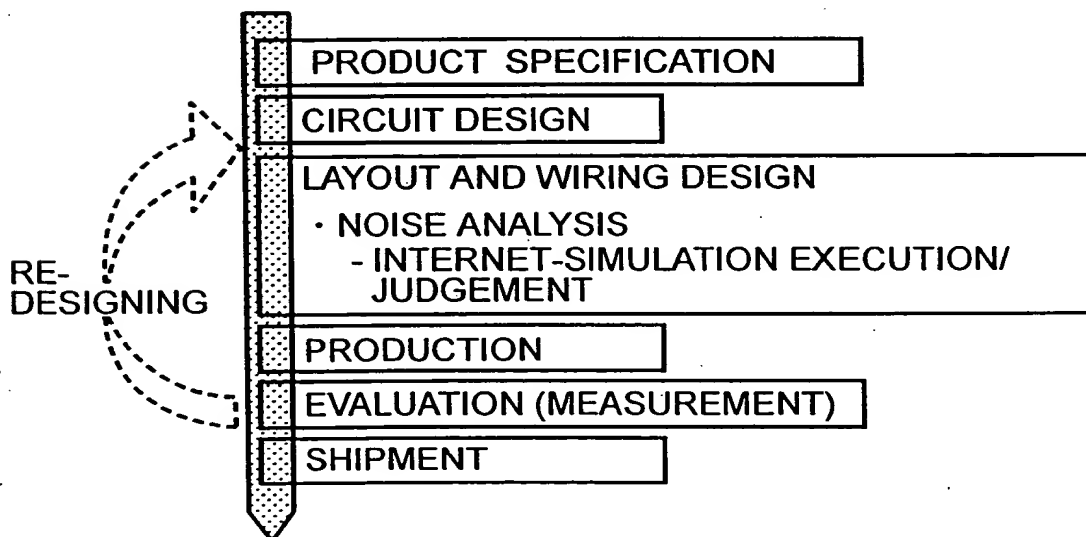
**FIG. 10(a)**

DESIGN FLOW AT CHIP-SET MANUFACTURER  
(CIRCUIT DESIGN ENGINEERING PARTY)



~~FIG. 10(a)~~ CONVENTIONAL DESIGN METHOD

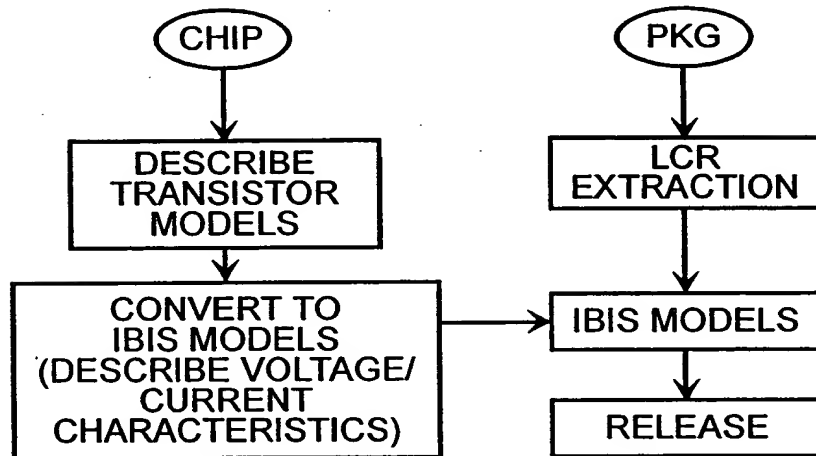
**FIG. 10(b)**



~~FIG. 10(b)~~ DESIGN METHOD ACCORDING TO THE  
PRESENT INVENTION

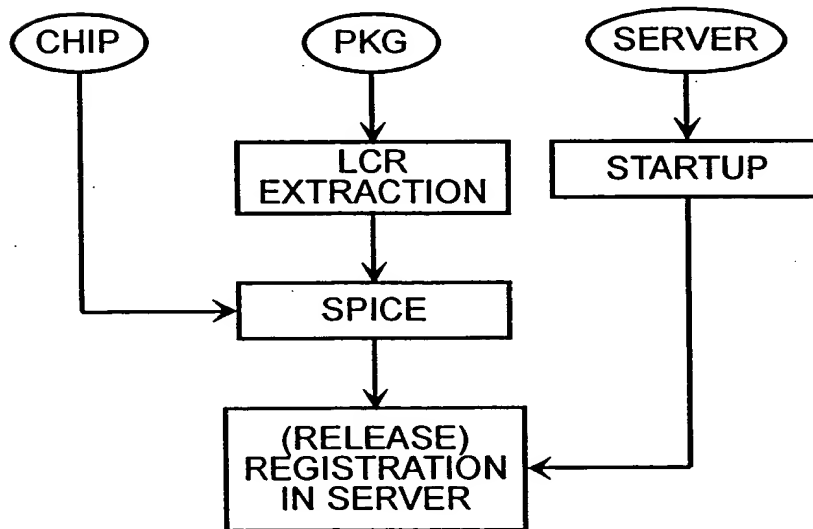
**FIG.11(a)**

MODEL PRODUCING FLOW AT MODEL SUPPLIER



~~CONVENTIONAL~~ CONVENTIONAL DESIGN METHOD

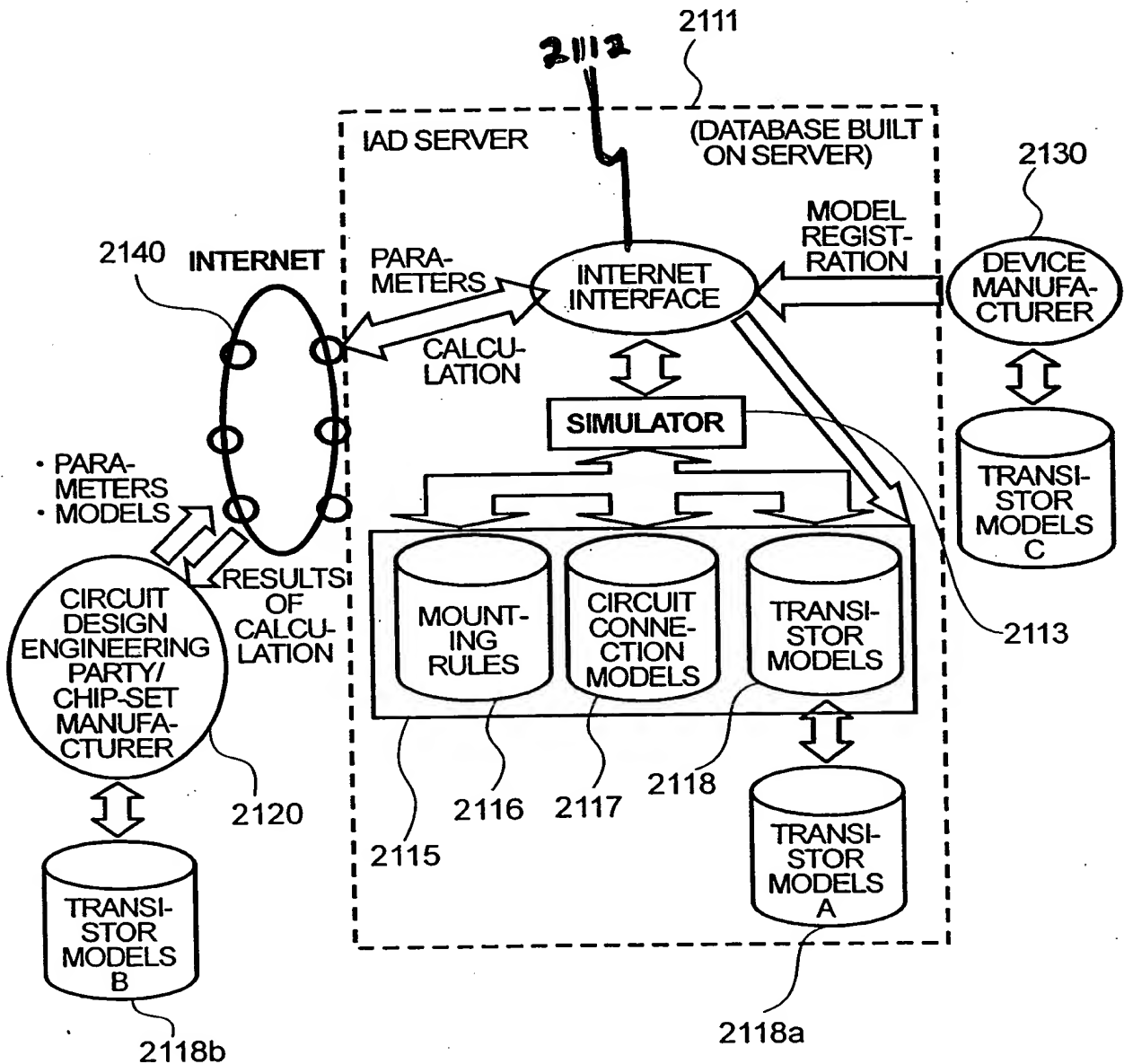
**FIG. 11(b)**



~~DESIGN METHOD~~ DESIGN METHOD ACCORDING TO THE PRESENT INVENTION

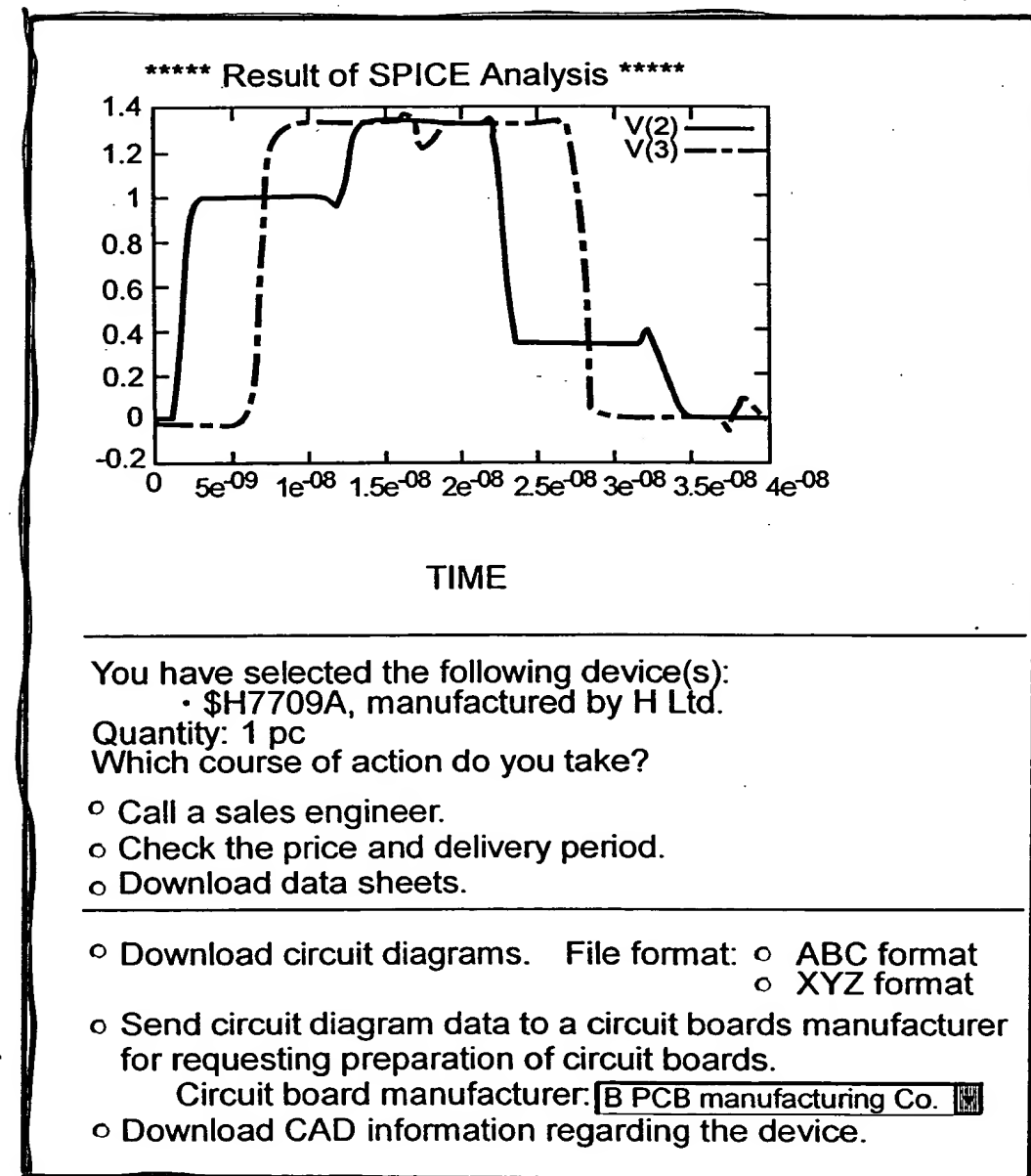
**FIG.12**

**SYSTEM CONFIGURATION IN A SECOND  
PREFERRED EMBODIMENT**



**FIG.14**

EXAMPLE OF CALCULATION RESULT AND  
DEVICE INFORMATION SCREEN



Approved  
for